We claim:

1. An apparatus comprising:

a first substrate;

a dielectric layer comprising a first dielectric material on said first substrate, said dielectric layer having a dielectric layer thickness and being traversed by through holes passing from an interface with said first substrate, to an opposite side of said dielectric layer; and

a second dielectric material at least partially blocking said through holes.

2. The apparatus of claim 1, comprising through holes having average diameters substantially smaller than an average spacing between mutually adjacent said through holes.

3. The apparatus of claim 1, in which said second dielectric material at least partially blocks a mutually adjacent pair of said through holes without forming a continuous layer between said mutually adjacent pair of through holes.

4. The apparatus of claim 1, in which said dielectric layer comprises pits that produce surface roughness in one surface of said dielectric layer, and wherein said second dielectric material at least partially fills said pits in a manner that reduces said roughness.

5. The apparatus of claim 1, in which said dielectric layer comprises bumps on one surface thereof, and areas surrounding said bumps are at least partially smoothed with said second dielectric material.

6. The apparatus of claim 1, in which said dielectric layer thickness is within a range of between about 10 nanometers and about 5 microns.

7. The apparatus of claim 1, in which said dielectric layer has a capacitance of at least about 5 nF/cm^2.

8. The apparatus of claim 1, further comprising a semiconductor layer on said dielectric layer.

9. The apparatus of claim 1, in which said first substrate is a conductor.

10. The apparatus of claim 1, further comprising a second substrate on said dielectric layer.

11. The apparatus of claim 8, further comprising a source electrode and a drain electrode in a spaced apart arrangement on said semiconductor layer.

12. A method of making an apparatus comprising a first substrate and a dielectric layer, comprising the steps of:

providing a first substrate;

providing a dielectric layer comprising a first dielectric material on said first substrate, said dielectric layer having a dielectric layer thickness and being traversed by through holes passing from an interface with said first substrate, to an opposite side of said dielectric layer; and

providing a second dielectric material that at least partially blocks said through holes.

13. The method of claim 12, comprising the further step of making said first substrate conductive while providing a second dielectric material.

14. The method of claim 12, comprising the further step of providing a reaction initiator on said first substrate prior to providing said dielectric layer, wherein the providing of said dielectric layer does not deactivate a portion of said reaction initiator located near entrances of said through holes.

15. The method of claim 12, comprising the further step of providing a reaction initiator on said opposite side of said dielectric layer.

16. The method of claim 12, further comprising the step of applying said second dielectric material to said opposite side of said dielectric layer while an electrical field is applied to said first substrate.

17. The method of claim 12, further comprising the step of forming a semiconductor layer on said dielectric layer.

18. The method of claim 12, in which said dielectric layer comprises pits and bumps that produce surface roughness in one surface of said dielectric layer, and wherein said second dielectric material at least partially fills said pits and at least partially smoothes areas surrounding said bumps in a manner that reduces said roughness.

19. The method of claim 12, in which said providing a dielectric layer produces a layer thickness within a range of between about 10 nanometers and about 5 microns.